EXHIBIT 16

U.S. Patent No. 6,871,264

Claim 1	Identification: Moto Edge[1]
1. A processor integrated circuit capable of executing more than one instruction stream comprising:	

View all specifications

performance

Operating System
Android™ 12 with easy access to the Google apps you use most

Internal Storage
128GB

Sensors
Proximity, Ambient Light, Accelerometer, Gyroscope, SAR Sensor, Magnetometer (compass), Barometer

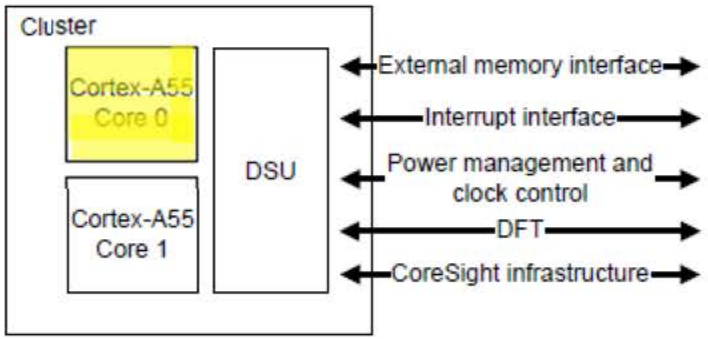
Processor
MediaTek Dimensity 1050

Memory (RAM)
6GB

Security
Fingerprint reader (on display)

[1] Additional infringing products include devices featuring ARM DynamIQ, sold or offered for sale by AT&T, including at least the Motorola Edge (2022), Edge 20, Edge 20 Pro, Edge 20 Lite, Edge (2021), Edge 20 Fusion, Google Pixel 5, and Google Pixel 4 devices.

Claim 1	Identification: Moto Edge[1]
	https://www.att.com/buy/phones/motorola-edge-2022.html https://www.motorola.com/us/smartphones-motorola-edge-gen-3/p?skuId=979 See also, https://www.gsmarena.com/motorola_edge_(2022)-11777.php **CPU** Architecture: 2x 2.5 GHz – Cortex-A78 6x 2 GHz – Cortex-A55 Cores: 8 Frequency: 2500 MHz Instruction set: ARMv8.2-A Process: 6 nanometers Manufacturing: TSMC https://nanoreview.net/en/soc/mediatek-dimensity-1050

Claim 1	Identification: Moto Edge[1]
a first processor, coupled to fetch instructions and access data through a first cache controller;	The Cortex-A55 core is a mid-range, low-power core that implements the ARMv8-A architecture with support for the v8.2 extension, the RAS extension, the Load acquire (LDAPR) instructions introduced in the ARMv8.3 extension, and the Dot Product instructions introduced in the ARMv8.4 extension. The core has a *Level 1* (L1) memory system, and private *Level 2* (L2) cache. The core is implemented inside the DynamIQ Shared Unit (DSU) as a Little core and is highly configurable with other cores. The following figure shows an example of a dual-core configuration.  **Figure A1-1 Example dual-core configuration with homogeneous cores** ARM® Cortex®-A55 Core, Revision r1p0, Technical Reference Manual

Claim 1	Identification: Moto Edge[1]
	A first processor (core) of the four ARM Cortex A-55 cores is coupled to fetch instructions and access data through a cache controller of its private L1I and L1D caches.
a second processor, coupled to fetch instructions and access data through a second cache controller;	

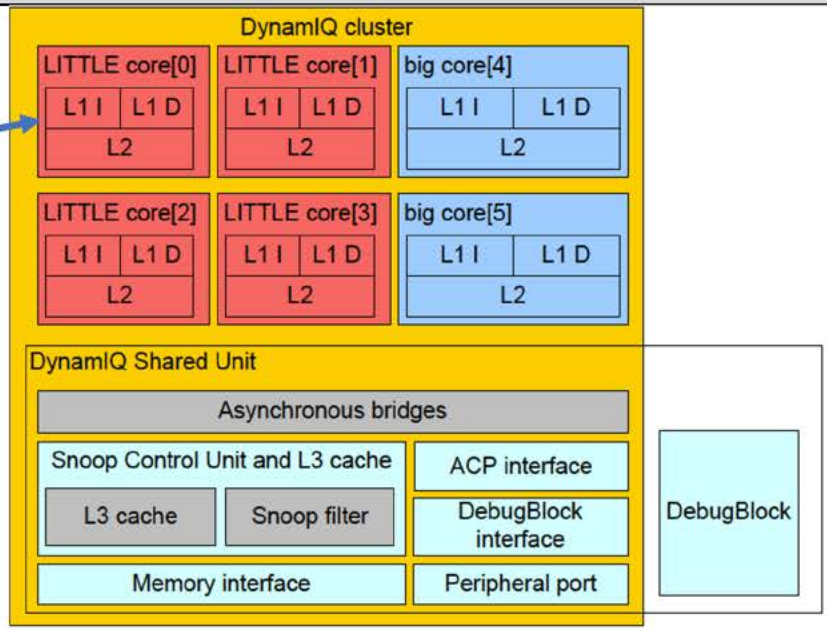


Figure A1-1 DynamIQ cluster

ARM® Cortex®-A55 Core, Revision r1p0, Technical Reference Manual, p. A1-26
Arm® DynamIQ™ Shared Unit, Revision r3p0, Technical Reference Manual, p. A1-20

Claim 1	Identification: Moto Edge[1]

A second processor (core) of the four ARM Cortex A-55 cores is coupled to fetch instructions and access data through a cache controller of its private L1I and L1D caches.

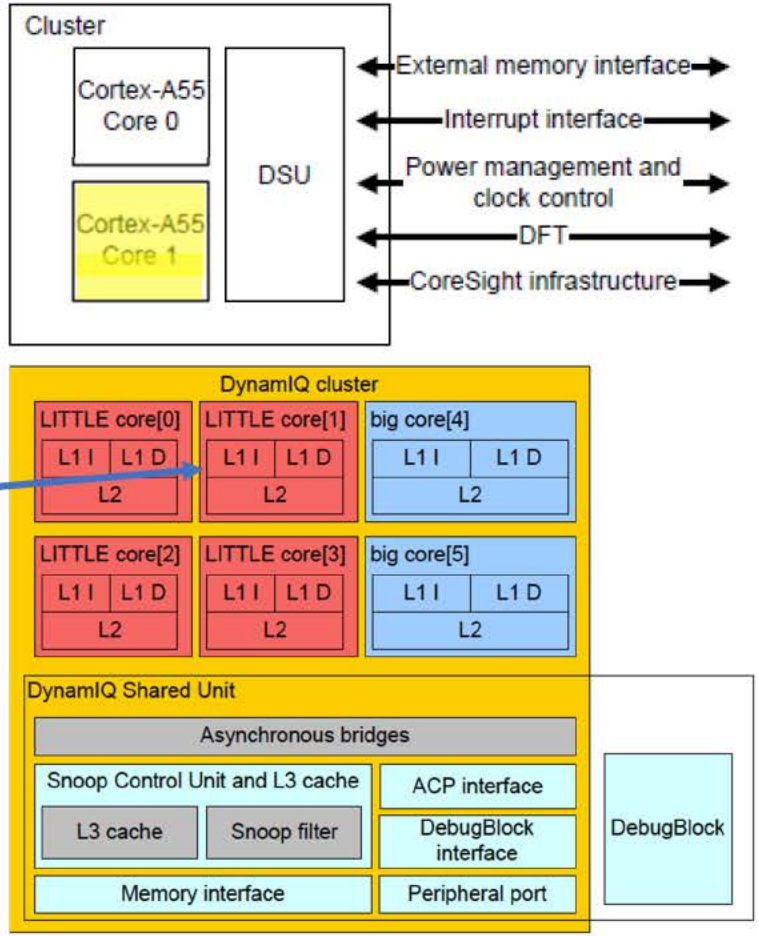


Figure A1-1 DynamIQ cluster

ARM® Cortex®-A55 Core, Revision r1p0, Technical Reference Manual, p. A1-26
Arm® DynamIQ™ Shared Unit, Revision r3p0, Technical Reference Manual, p. A1-20

Claim 1	Identification: Moto Edge[1]
a plurality of cache memory blocks;	A plurality of cache memory blocks exists in the L3 cache shared by all ARM cores in a DynamIQ cluster and partitioned into groups of 4 cache ways (blocks).

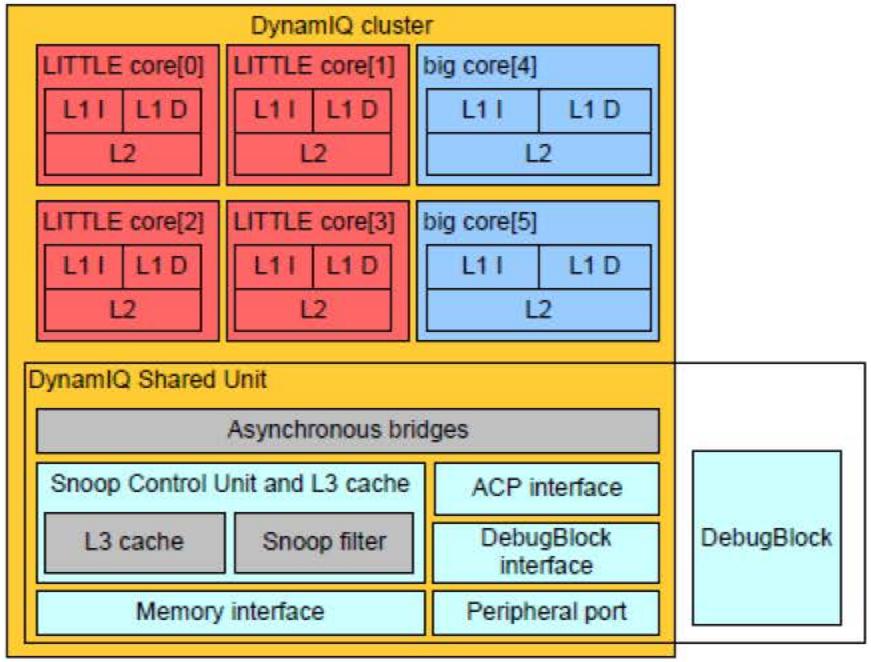
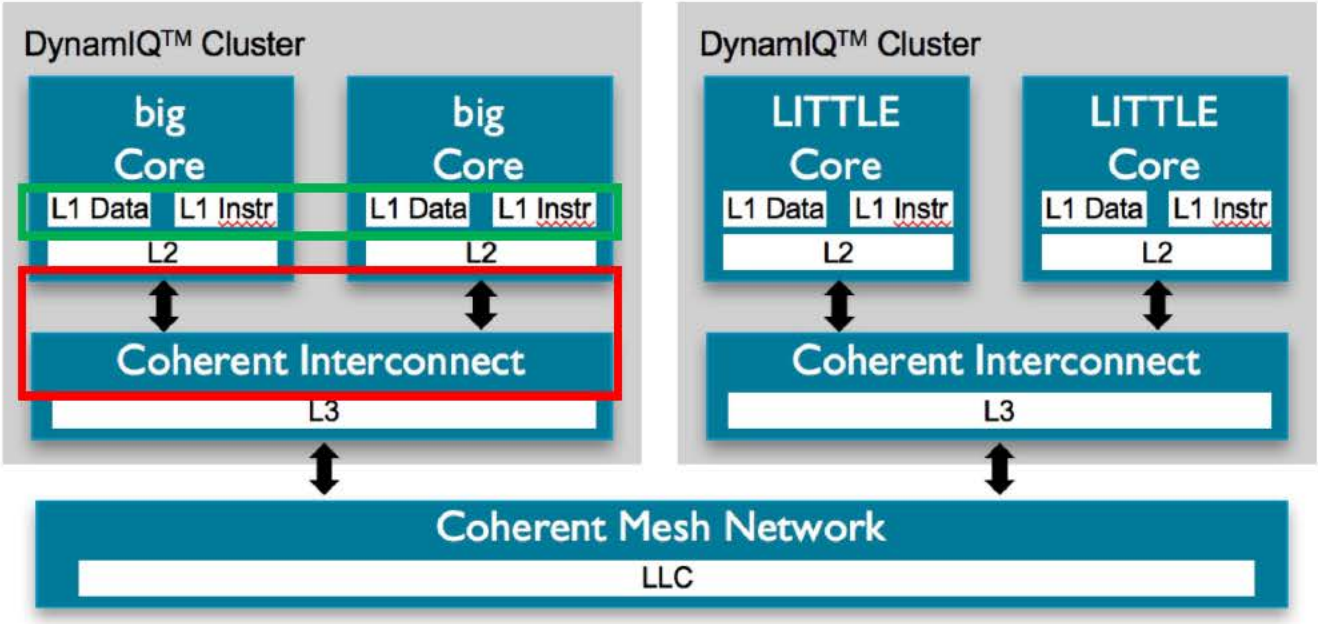


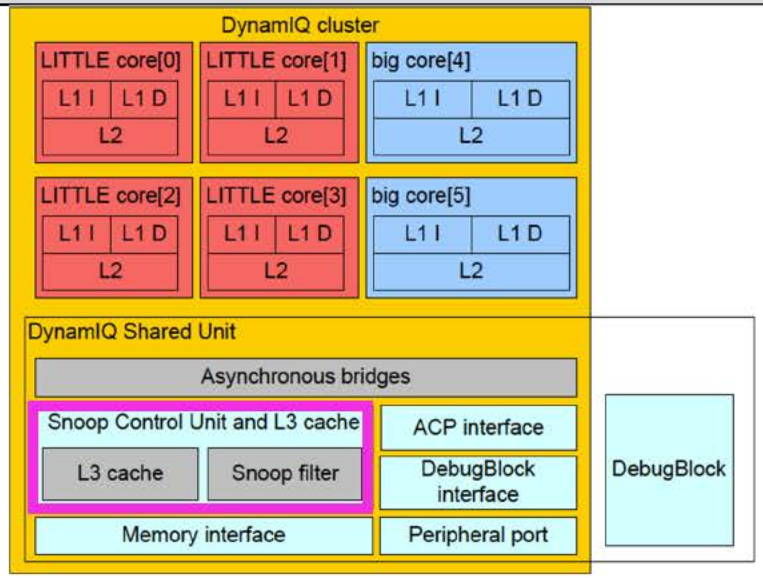
Figure A1-1 DynamIQ cluster

Within the DSU, the L3 cache, the *Snoop Control Unit* (SCU), internal interfaces to the cores, and external interfaces to the SoC are present.

Arm® DynamIQ™ Shared Unit, Revision r3p0, Technical Reference Manual, p. A1-20

Claim 1	Identification: Moto Edge[1]
	About the L3 cache The optional L3 cache is shared by all the cores in the cluster. The L3 cache supports a dynamically optimized allocation policy. Groups of cache ways can be partitioned and assigned to individual processes, allowing cache allocation to be fairly shared between processes. Arm® DynamIQ™ Shared Unit, Revision r3p0, Technical Reference Manual, p. A5-64
a high-speed interconnect coupling the plurality of cache memory blocks to the first and second cache controllers such that at least one allocable cache memory block is capable of being used by the first and second cache controllers; and	A high-speed interconnect (e.g., Coherent Interconnect) couples the cache memory blocks of shared L3 cache to the first and second cache controllers (e.g., of the L1D and L1I caches of the first and second cores). **L3 cache allocation policy** The L3 cache data allocation policy changes depending on the pattern of data usage. *Exclusive allocation* is used when data is allocated in only one core. Inclusive allocation is used when data is shared between cores. For example, an initial request from core 0 allocates data in the L1 or L2 caches but is not allocated in the L3 cache. When data is evicted from core 0, the evicted data is allocated in the L3 cache. The allocation policy of this cache line is still exclusive. If core 0 refetches the line, it is allocated in the L1 or L2 caches of core 0 and removed from the L3 cache, keeping the line exclusive. If core 1 then accesses the line for reading, it remains cached in core 0 and is also allocated in both core 1 and L3 caches. In this case, the line has inclusive allocation. Arm® DynamIQ™ Shared Unit, Revision r3p0, Technical Reference Manual, p. A5-65

Claim 1	Identification: Moto Edge[1]
	 https://community.arm.com/developer/ip-products/system/b/soc-design-blog/posts/using-portable-stimulus-in-the-arm-world-creating-bare-metal-sw-coherency-scenarios
a resource allocation controller coupled to determine an accessing cache memory controller selected from the group consisting of the first and second cache memory controllers, whereby the accessing	A resource allocation controller (e.g., part of the Snoop Control Unit and L3 cache) is coupled (e.g., to the CLUSTERPARTCR register) to determine an accessing cache memory controller selected from the first and second cache controllers, whereby the accessing cache memory controller is allowed to access the allocable cache memory block (in shared L3 cache).

Claim 1	Identification: Moto Edge[1]
cache memory controller is allowed to access the allocable cache memory block, wherein the cache memory blocks are usable by the cache controllers to store data and instructions fetched from a random-access memory.	 **Figure A1-1 DynamIQ cluster** **About the L3 cache** The optional L3 cache is shared by all the cores in the cluster. The L3 cache supports a dynamically optimized allocation policy. Groups of cache ways can be partitioned and assigned to individual processes, allowing cache allocation to be fairly shared between processes.

Claim 1	Identification: Moto Edge[1]
	L3 cache partitioning The L3 cache supports a partitioning scheme that alters the victim selection policy to avoid one core (or one group of cores) from utilizing the entire cache at the expense of another core. Cache partitioning is intended for specialized software where there are distinct classes of processes running with different cache accesses patterns. For example, two processes (A and B) run on separate cores in the same cluster and therefore share the L3 cache. If process A is more data-intensive than process B, process A might cause all cache lines allocated by process B to be evicted. In this case, the performance of process B might be reduced. In use, each core in the cluster must be assigned to one of the eight partition scheme IDs. The partitioning is done in groups of cache ways. Each group contains four cache ways. A group can be assigned as private to one or more scheme IDs, or it can be left unassigned. An unassigned group can be shared between all scheme IDs. Accesses from a given core can allocate into any cache way that is assigned as private to that core's partition scheme ID, or to any cache way that is shared. Arm® DynamIQ™ Shared Unit, Revision r3p0, Technical Reference Manual, pp. A1-20, A5-64, A5-66

CLUSTERPARTCR, Cluster Partition Control Register

The CLUSTERPARTCR register controls a group of ways to be marked as private to a scheme ID. This register is RW.

This description applies to both the AArch32 (CLUSTERPARTCR) and AArch64 (CLUSTERPARTCR_EL1) registers.

Bit field descriptions

CLUSTERPARTCR is a 32-bit register, and is part of SCU and L3 cache configuration registers.

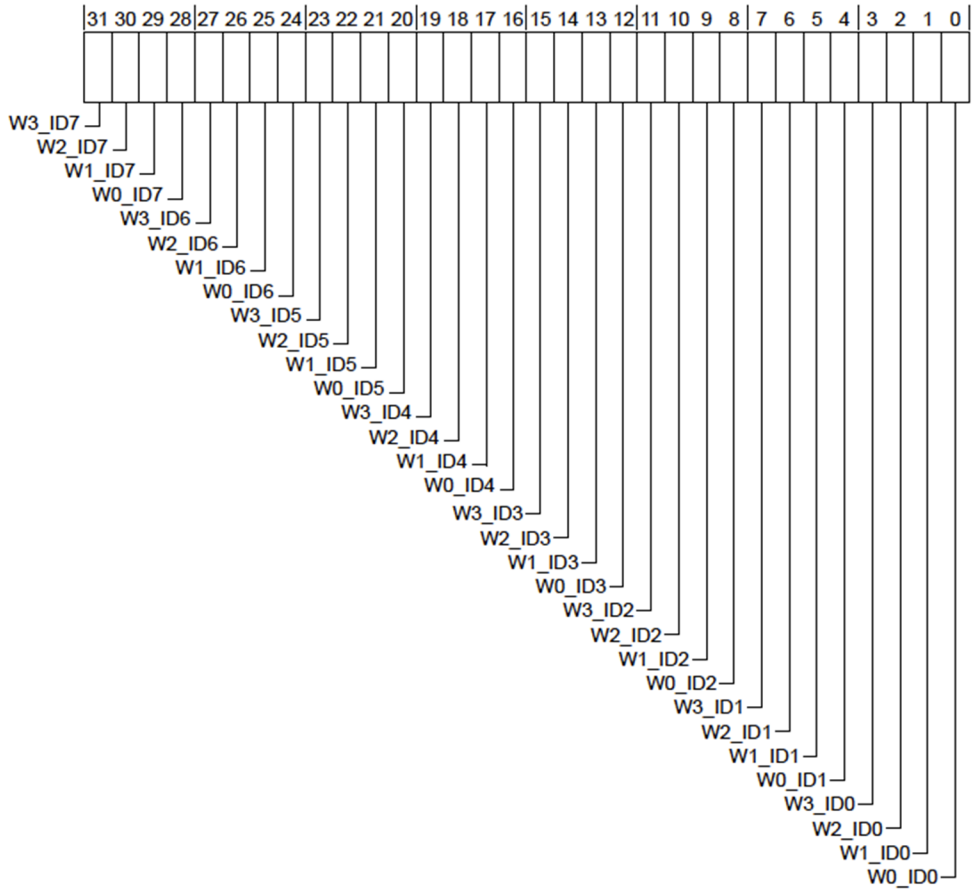


Figure B1-8 CLUSTERPARTCR bit assignments

Claim 1	Identification: Moto Edge[1]

Each bit, if set, indicates that a group of four ways is allocated as private to that scheme ID. If more than one scheme ID assigns the same group of ways as private, then those ways are shared between the scheme IDs that have assigned them as private. All ways not assigned to any scheme ID are treated as shared between all scheme IDs. If a scheme ID does not have any private ways allocated, and there are no remaining shared ways, then any use of the scheme ID will allocate to way group 0, as this is considered a programming error.

Arm® DynamIQ™ Shared Unit, Revision r3p0, Technical Reference Manual, p. B1-132

The Lenovo Tab P12 Pro comes with 6/8 GB of RAM

Specifications

Processor	Qualcomm Snapdragon 870
Operating system	Android 11 (Upgradable to Android 12L)
Memory	6/8GB of RAM, 128/256GB of storage, expandable up to 1TB via MicroSD
Display	12.6-inch, 2K (2,560 x 1,600) OLED panel with 120Hz
Brightness	600 nits
Battery	10,200mAh, 30W charging
Camera	13MP rear camera (auto-focus) with a 5MP wide angle, 8MP front (fixed-focus)
Connection ports	Micro USB-C 2.0, 4-point Pogo pins, keyboard connector slots, MicroSD card slot, stylus port